ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

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Title of Invention	Integrated Redundancy Architecture and Method for Providing Redundancy Allocation to an Embedded Memory System

Application Number :

Confirmation Number:

First Named Applicant: Wayne Ellis

Attorney Docket Number: BUR920030151US1

Art Unit:

Examiner:

Search string: (6574757 or 6408401 or 5764878 or 20030123301 or 20030028710 or 20020196680).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
/GM/	1	6574757	2003-06-03	Park et al.		714	710
/GM/	2	6408401	2002-06-18	Bhavsar et al.		714	7
/GM/	3	5764878	1998-06-09	Kablanian et al.		395	182.05

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
/GM/	1	20030123301	2003-07-03	Jang et al.		365	200
/GM/	2	20030028710	2003-02-06	Shinohara et al.		711	104
/GM/	3	20020196680	2002-12-26	Ooishi et al		365	200

Signature

Examiner Name	Date
/Guerrier Merant/	08/13/2007